What is claimed is:

B7 1. A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate,

wherein a spacing between a fist gate electrode of the first MOS transistors constituting the input circuit or the output circuit and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, and

wherein a spacing between a second gate electrode of the second MOS transistors constituting the internal circuit and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact hole.

2. A semiconductor device including an input circuit or an output circuit configured with a plurality of first MOS transistors in a first area of a principal plane on a

semiconductor substrate, and an internal circuit configured with a plurality of second MOS transistors in a second area of the principal plane on the semiconductor substrate,

wherein a spacing between an edge of a first active region in which the first MOS transistors constituting the input circuit or the output circuit are formed and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the edge of the first active region and the first contact hole, and

wherein a spacing between an edge of a second active region in which the second MOS transistors constituting the internal circuit are formed and a second contact hole for connecting a wiring to a source or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the edge of the second active region and the second contact hole.

3. A semiconductor device according to Claim 1 or Claim 2, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is equal to a power supply voltage applied to the second MOS transistors constituting the internal circuit.

4. A semiconductor device according to Claim 2 or Claim 3, wherein a gate length of the first MOS transistors is equal to a gate length of the second MOS transistors.

5. A semiconductor device according to Claim 3, wherein a gate insulating film thickness of the first MOS transistors is equal to a gate insulating film thickness of the second MOS transistors.

6. A semiconductor device according to Claim 3, wherein an area of the active region in which the first MOS transistors are formed is larger than an area of the active region in which the second MOS transistors are formed.

7. A semiconductor device according to Claim 1 or Claim 2, wherein a power supply voltage applied to the first MOS transistors constituting the input circuit or the output circuit is higher than a power supply voltage applied to the second MOS transistors constituting the internal circuit.

8. A method of manufacturing a semiconductor device having plural processes for forming plural types of MOS transistors to which different power supply voltages are applied in correspondence with external power supply voltages,

wherein the plural processes are comprised of a process common to the plural types of MOS transistors and a process different by each of the plural types of MOS transistors.

9. A method of manufacturing a semiconductor device according to Claim 8, wherein the plural processes are comprised of a first process common to the plural types of MOS transistors, a second process following the first process, which is different by each of the plural types of MOS transistors, and a third process following the second process, which is common to the plural types of MOS transistors.

10. A method of manufacturing a semiconductor device according to Claim 9, wherein the second process includes a process that forms plural types of gate insulating films of which thickness are different from each other.

11. A method of manufacturing a semiconductor device according to Claim 9, wherein the second process includes a process that forms plural types of gate electrodes of which gate lengths are different from each other.

12. A method of manufacturing a semiconductor device according to Claim 11, wherein areas of active regions where

the plural types of gate electrodes are formed are equal to each other.

13. A method of manufacturing a semiconductor device according to Claim 9, wherein the second process includes a process that forms plural types of channel formed areas of which impurity concentrations are different from each other.

14. A method of manufacturing a semiconductor device according to Claim 9, wherein the first process includes a process that forms a well on the semiconductor substrate.

15. A method of manufacturing a semiconductor device according to Claim 8, wherein the plural types of MOS transistors are MOS transistors that constitute an input circuit or an output circuit.

16. A method of manufacturing a semiconductor device comprising the steps of:

forming a first semiconductor device configured with a plurality of first MOS transistors, which includes an input circuit or an output circuit supplied with a first external supply voltage, on a principal plane of a first semiconductor wafer, and

forming on the principal plane of a second semiconductor wafer a second semiconductor device configured with a plurality of second MOS transistors, including an input circuit or an output circuit supplied with a second external supply voltage different from the first external supply voltage, which has the same function as the first semiconductor device,

wherein the plural processes that form the first MOS transistors on the principal plane of the first semiconductor wafer, and the plural processes that form the second MOS transistors on the principal plane of the second semiconductor wafer are comprised of a first process common to the first and second MOS transistors, a second process following the first process, which is different in the first MOS transistors and the second MOS transistors, and a third process following the second process, which is common to the first and second MOS transistors.

17. A method of manufacturing a semiconductor device according to Claim 16, wherein the second process includes a process that forms two types of gate insulating films of which thickness are different from each other.

18. A method of manufacturing a semiconductor device according to Claim 16, wherein the second process includes a

process that forms two types of gate electrodes of which gate lengths are different from each other.

19. A method of manufacturing a semiconductor device according to Claim 16, wherein the second process includes a process that forms two types of channel formed areas of which impurity concentrations are different from each other.

20. A method of manufacturing a semiconductor device according to Claim 16,

wherein an area of a first active region where the first MOS transistors are formed is equal to an area of a second active region where the second MOS transistors are formed,

wherein a spacing between a fist gate electrode of the first MOS transistors and a first contact hole for connecting a wiring to a source region or a drain region of the first MOS transistors is larger than a minimum processing dimension of the spacing between the first gate electrode and the first contact hole, and

wherein a spacing between a second gate electrode of the second MOS transistors and a second contact hole for connecting a wiring to a source region or a drain region of the second MOS transistors is equal to a minimum processing dimension of the spacing between the second gate electrode and the second contact

hole.